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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,840	SUH, JUNGWON	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-29,31,32,38 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32,38 and 39* is/are allowed.

6)☒ Claim(s) *1-10,15-29, 31* is/are rejected.

7)☒ Claim(s) *11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 7-9, 15,16, 20-29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Moroni et al. (U. S. PAT. 5,606,531).

In claim 1, Moroni et al. teaches all claimed features in Fig. 3, a clock stop detector for a memory for detecting a clock signal being not active (when clock signal 14 is at logic 0) for a predetermined period of time (a certain time period), the clock stop detector comprising: a first switch (M5) that closes in response to a first logic level (logic 0) of an inverted clock signal (output from 15) to charge a capacitor (C2); a second switch (M6) that closes (conducting) in response to a second logic level (logic 1) of the clock signal to discharge the capacitor; and a logic circuit (16) that receives the clock signal (14 via node A) and a charge signal (charged C2) based on a charge (voltage level) on the capacitor, and that outputs a control signal (11) indicating when the clock signal was not active (when 14 was at logic low) for a period of time (half cycle of the clock) exceeding (greater or longer than the certain time period) the predetermined period of time, wherein the capacitor (C2) is charged to the second logic level (the logic 1 or Vcc) when the inverted clock signal (the output from 15 is at logic 0) is at the first

logic level, and wherein the capacitor is discharged to the first logic level (to logic 0 or ground) when the inverted clock signal is at the second logic level for a period of time (a second half cycle of the clock) exceeding the predetermined period of time.

In claims 2 and 3, Moroni et al. further teaches the clock stop detector of claim 1, wherein the first switch comprises a first transistor (M5) and the second switch comprises a second transistor (M6); and wherein the first transistor is a p-type metal-oxide semiconductor field effect transistor (pMOS) and the second transistor is an n-type metal-oxide semiconductor field effect transistor (nMOS).

In claims 5, 7 and 8, Moroni et al. further teaches the clock stop detector of claim 1, wherein the first logic level is a logic low logic level (logic 0) and the second logic level is a logic high logic level (1); a power supply voltage (Vcc) coupled to the first switch (M5) to charge the capacitor (C2) if the first switch is closed (logic 0); and wherein the second switch (M6) is open (logic 0) if the first switch is closed and the first switch is open if the second switch is closed.

In claim 9, Moroni et al. teaches all claimed features in Figs. 1 and 3, a memory comprising: a clock stop detector (2) for detecting a clock signal being not active (when clock signal 14 is at logic 0) for a predetermined period of time (a certain time period), the clock stop detector configured to receive the clock signal (CK) and output a control signal (11) in response to the clock signal (CK) and a peripheral circuit (3) for reading and writing data (via 7) to a memory bank (5), wherein the peripheral circuit is configured to receive the control signal (via 8) and activate and deactivate in response to the control signal, wherein the clock stop detector comprising: a first switch (M5) that

closes in response to a first logic level (logic 0) of an inverted clock signal (output from 15) to charge a capacitor (C2); a second switch (M6) that closes (conducting) in response to a second logic level (logic 1) of the clock signal to discharge the capacitor; and a logic circuit (16) that receives the clock signal (14 via node A) and a charge signal (charged C2) based on a charge (voltage level) on the capacitor, and that outputs a control signal (11) indicating when the clock signal was not active (when 14 was at logic low) for a period of time (half cycle of the clock) exceeding (greater or longer than the certain time period) the predetermined period of time, wherein the capacitor (C2) is charged to the second logic level (the logic 1 or Vcc) when the inverted clock signal (the output from 15 is at logic 0) is at the first logic level, and wherein the capacitor is discharged to the first logic level (to logic 0 or ground) when the inverted clock signal is at the second logic level for a period of time (a second half cycle of the clock) exceeding the predetermined period of time.

In claim15, Moroni et al. further teaches in Fig. 3, the memory of claim 9 wherein the first switch comprises a first transistor (M5) and the second switch comprises a second transistor (M6).

In claim 16, Moroni et al. further teaches in Fig. 1, the memory of claim 9 wherein the memory comprises a random access memory (4).

Claims 20 and 21 correspond to detailed circuitry already discussed similarly with regard to claims 9 and 16.

Method claims 22-28 correspond to detailed circuitry already discussed similarly with regard to claims 1-3, 5, 7 and 8.

In claim 29, Moroni et al. teaches all claimed features in Figs. 1-3, a portable electronic device comprising: a controller (1) configured to output a clock signal (10) that starts and stops in response to user commands (EXT-RST) to a portable electronic device (not shown); and a memory (4 or 5) that receives the clock signal (via 7), the memory comprising: a clock stop detector (2) configured to output a clock stop signal (11) in response to the clock signal being not active for a predetermined period of time (logic 0 for a certain period of time); a peripheral circuit (3) configured to receive the clock stop signal (via 8) and activate and deactivate in response to the clock stop signal; and a memory bank (5) configured to receive address signals (via 7), control signals (via 7), and data signals (via 7) from the peripheral circuit for reading and writing data in the memory bank, wherein the clock stop detector comprising: a first switch (M5) that closes in response to a first logic level (logic 0) of an inverted clock signal (output from 15) to charge a capacitor (C2); a second switch (M6) that closes (conducting) in response to a second logic level (logic 1) of the clock signal to discharge the capacitor; and a logic circuit (16) that receives the clock signal (14 via node A) and a charge signal (charged C2) based on a charge (voltage level) on the capacitor, and that outputs a control signal (11) indicating when the clock signal was not active (when 14 was at logic low) for a period of time (half cycle of the clock) exceeding (greater or longer than the certain time period) the predetermined period of time, wherein the capacitor (C2) is charged to the second logic level (the logic 1 or Vcc) when the inverted clock signal (the output from 15 is at logic 0) is at the first logic level, and wherein the capacitor is discharged to the first logic level (to logic 0 or ground) when the inverted clock signal is

at the second logic level for a period of time (a second half cycle of the clock) exceeding the predetermined period of time.

In claim 31, Moroni et al. further teaches the memory of claim 29, wherein the portable electronic device comprises one of a cellular telephone, a personal digital assistant, a music player, a game system, a digital camera, and a computer (1 is a computer).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moroni et al. in view of Nakashima (U. S. PAT. 5,517,144).

In claim 4, Moroni et al. teaches all claimed features of claim 1, with the exception of teaching wherein the logic circuit comprises a NOR gate. However, Nakashima teaches in Fig. 2, the logic circuit (16) comprises a NOR gate (19).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Moroni et al. with the teachings of Nakashima in order to provide a power-on reset circuit that generates a reset signal with stability without affected by a rising characteristic of a power-supply voltage.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moroni et al. in view of Forbes (U. S. PAT. 6,649,476).

In claim 6, Moroni et al. teaches all claimed features of claim 1, with the exception of teaching a current source coupled to the second switch to discharge the capacitor if the second switch is closed. However, Forbes teaches in Fig. 1, a current source (16) coupled to the second switch (20) to discharge the capacitor (not marked) if the second switch is closed.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Moroni et al. with the teachings of Forbes in order to provide a circuit that monitors the clock signal and if the irregularity is detected, generates a reset signal holding the microprocessor in a safe state.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moroni et al. in view of Ooishi (U. S. PAT. 6,246,614).

In claim 10, Moroni et al. teaches the memory of claim 9; with the exception of teaching a clock receiver configured to receive an external clock signal and pass the clock signal to the clock stop detector. However, Ooishi teaches all claimed features in Fig. 1, a clock receiver (2) configured to receive an external clock signal (CLK) and pass the clock signal to the clock stop detector (5).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Moroni et al. with the teaching of Ooishi in order to buffer and condition an external clock and outputting an output clock signal to the clock stop detector circuit.

8. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moroni et al.

In claim 17, Moroni et al. teaches the memory of claim 9; with the exception of teaching wherein the memory comprises a dynamic random access memory. However, it is obvious to one ordinary skill in the art to select a dynamic random access memory for the memory because the dynamic random access memory equipped with synchronous clock.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to select a dynamic random access memory for the memory in order to synchronize data during read/write operation.

In claim 18, Moroni et al. teaches the memory of claim 9; with the exception of teaching wherein the memory comprises a double data rate synchronous dynamic random access memory. However, it is obvious to one ordinary skill in the art to select a double data rate synchronous dynamic random access memory because it operates on both edges of the clock signal; thus high-speed operation can be achieved.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to select a double data rate synchronous dynamic random access memory for the memory in order to accurately synchronize data during read/write operation with high-speed.

In claim 19, Moroni et al. teaches the memory of claim 9, with the exception of teaching wherein the memory comprises a mobile random access memory. However, it is obvious to one ordinary skill in the art to select a mobile random memory for memory

because mobile random memory requires low power to operate; thus it is suitable for hand-held electronic devices.

9. Claims 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 32, 38 and 39 appear to comprise allowable subject matter.

Response to Arguments

11. Applicant's arguments with respect to claims 1, 9, 20, 22 and 29 have been considered but are moot in view of the new ground(s) of rejection.

The applied reference of Moroni et al. still anticipates applicant's claimed invention of claims 1-3, 5, 7-9, 15, 16, 20-29 and 31; claim 4 is rejected as being unpatentable over the combination of Moroni in view of Nakashima; claim 6 is rejected as being unpatentable over the combination of Moroni in view of Forbes; claim 10 is rejected as being unpatentable over the combination of Moroni in view Ooishi; and claims 17-19 are rejected as being unpatentable over Moroni.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER